This listing of the claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claims 1-20 (Cancelled).

Claim 21 (Currently Amended) A semiconductor structure comprising:

a first semiconductor active area having, and laterally surrounded by, a first sidewall and located in a semiconductor substrate;

a first trench isolation region laterally abutting said first sidewall and surrounding said first semiconductor active area and comprising silicon oxide, wherein a first portion of a bottom surface of said first trench isolation region and said first sidewall does not contact any nitride liner;

a second semiconductor active area having, and laterally surrounded by, a second sidewall and located in said semiconductor substrate;

a nitride liner laterally abutting said second sidewall and a second portion of said first trench isolation region, wherein said second portion laterally abuts said first portion, and wherein an edge of said nitride liner is located at a bottom surface of said first trench isolation region underneath a boundary between said first portion and said second portion; and

a second trench isolation region laterally abutting said nitride liner and surrounding said second semiconductor active area and comprising silicon oxide, wherein another edge of said nitride liner is located at a bottom surface of said second trench isolation region.

Claim 22 (Previously Amended) The semiconductor structure of Claim 21, wherein said first semiconductor active area is under a first compression stress and said second semiconductor active area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 23 (Previously Amended) The semiconductor structure of Claim 21, wherein said nitride liner is present on the entirety of said second sidewall surrounding said second semiconductor active area.

Claim 24 (Previously Amended) The semiconductor structure of Claim 21, wherein any bird's beak structure comprising a dielectric material and having a taper in lateral width is absent between said first semiconductor active area and said first trench isolation region.

Claim 25 (Previously Amended) The semiconductor structure of Claim 21, further comprising at least one bird's beak structure including a dielectric material and having a taper in lateral width and located between said second semiconductor active area and said second trench isolation region.

Claim 26 (Previously Amended) The semiconductor structure of Claim 21, further comprising at least one bird's beak structure comprising a dielectric material and having a taper in lateral width and located between said second semiconductor active area and said second trench isolation region, wherein any bird's beak structure comprising a dielectric material and having a taper in

lateral width is absent between said first semiconductor active area and said first trench isolation region.

Claim 27 (Previously Amended) The semiconductor structure of Clam 21, wherein said first semiconductor active area includes at least one PFET and said second semiconductor active area includes at least one NFET.

Claim 28 (Cancelled).

Claim 29 (Previously Presented) The semiconductor structure of Claim 21, wherein said nitride liner is a nitride surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 30 (Previously Presented) The semiconductor structure of Claim 21, wherein a nitride liner is present on at least a portion of a bottom of said first trench isolation region.

Claim 31 (Previously Presented) The semiconductor structure of Claim 21, wherein at least a portion of a bottom of said second trench isolation region is void of any nitride liner.

Claim 32 (Currently Amended) A semiconductor structure comprising:

a trench isolation region located in a semiconductor substrate;

a first semiconductor active area having, and laterally surrounded by, a first sidewall that laterally abuts said trench isolation region and is located in said semiconductor substrate, wherein said first sidewall does not contact any nitride liner;

a second semiconductor active area having, and laterally surrounded by, a second sidewall and located in said semiconductor substrate; and

a nitride liner laterally abutting said second sidewall and said trench isolation region wherein an edge of said nitride liner is located at a bottom surface of said trench isolation region.

Claim 33 (Previously Amended) The semiconductor structure of Claim 32, wherein said first semiconductor active area is under a first compression stress and said second semiconductor active area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.

Claim 34 (Previously Presented) The semiconductor structure of Claim 32, wherein the entirety of said first sidewall is void of any nitride liner and said nitride liner is present on the entirety of said second sidewall.

Claim 35 (Previously Amended) The semiconductor structure of Claim 32, wherein any bird's beak structure including a dielectric material and having a taper in lateral width is absent between said first semiconductor active area and said first trench isolation region.

Claim 36 (Previously Amended) The semiconductor structure of Claim 32, further comprising at least one bird's beak structure including a dielectric material and having a taper in lateral width and is located between said second semiconductor active area and said second trench isolation region.

Claim 37 (Previously Amended) The semiconductor structure of Clam 32, wherein said first semiconductor active area includes at least one PFET and said second semiconductor active area includes at least one NFET.

Claim 38 (Cancelled).

Claim 39 (Previously Presented) The semiconductor structure of Claim 32, wherein said nitride liner is a nitrided surface layer that has a thickness of about 0.1 nm to about 2.0 nm.

Claim 40 (Previously Presented) The semiconductor structure of Claim 32, wherein said first sidewall does not adjoin said second sidewall.

Claim 41 (New) A semiconductor structure comprising:

a trench isolation region located in a semiconductor substrate;

a first semiconductor active area having, and laterally surrounded by, a first sidewall that laterally abuts said trench isolation region and is located in said semiconductor substrate, wherein said first sidewall does not contact any nitride liner;

a second semiconductor active area having, and laterally surrounded by, a second sidewall and located in said semiconductor substrate; and

a nitride liner laterally abutting said second sidewall and said trench isolation region and abutting a semiconductor material of said second semiconductor active area.

Claim 42 (New) The semiconductor structure of Claim 41, wherein said first semiconductor active area is under a first compression stress and said second semiconductor active area is under a second compression stress and the level of first compression stress is higher than the level of second compression stress.